

# Tech Briefing 2023

December 2023

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# Efforts toward Zero Defect Packaging

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- What is the Mid-Process Research Center?
- Highly-Reliable Processes  
(Maximized Process Performance)
- No Variation (Automated)
- Summary

- **Purpose of Establishment**

- As the wafers on which circuits are built in the front-end process of semiconductor manufacturing have extremely high added-value, high yield is required in the processes that follow. Among these processes, in the grinding (wafer thinning) and dicing (wafer singulation through cutting) processes handled by DISCO, there is a risk that one processing failure may cause the entire wafer's quality to deteriorate. Therefore, caution and accuracy are required for operations such as processing and transfer in particular. In addition, if a large number of defects occur in the back-end process, most of the time, alternative wafers cannot immediately be supplied from the front-end process. As a result, this may have a significant impact on the entire supply chain and become a large issue in the lean manufacturing of the automotive industry. Recognizing these issues, DISCO has newly positioned these processes that are conventionally in the back-end process of semiconductor manufacturing as part of the "mid-process" and has been proceeding with R&D in this area.
- DISCO has officially established the mid-process research center as a site to conduct R&D for the mid-process and perform demonstrations for customers. This center has permanent installations of the wafer transfer system RoofWay as well as the cluster system MUSUBI, and research is underway to reduce the equipment operator's responsibilities and improve semiconductor wafer processing and transfer quality through automation of the production system.
- As semiconductor use in automotive applications is increasing, stricter quality management is being required for semiconductors as well, as they are responsible for the user's life. Therefore, through this center, DISCO will aim at realizing a production system that eliminates operator intervention as much as possible in order to reduce quality variation that arises from human involvement.

## Concept

### **Automotive Devices**

**Demand for stricter quality management**



### **Zero Defects**

**No variation in quality**

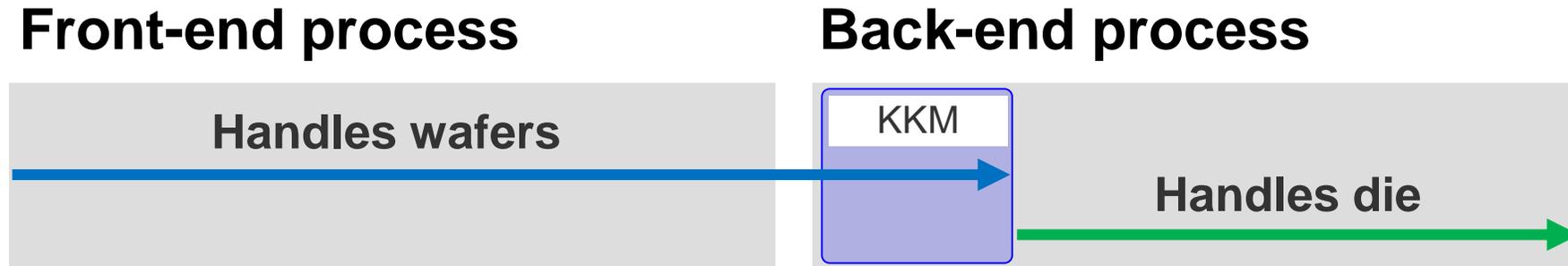
**In order to realize this, we need**

**Maximized process  
performance**

**+ Automation**

**Both are required!**

**KKM is situated within the back-end process but transfers wafers rather than die**



**Processing failure causes entire wafer quality to deteriorate.**

- ▶ **Caution and accuracy are required for operations such as processing and transfer in particular.**

**Grinding and dicing, conventionally included in the back-end process, are positioned as part of the “mid-process.”**

## Four elements of CR production automation

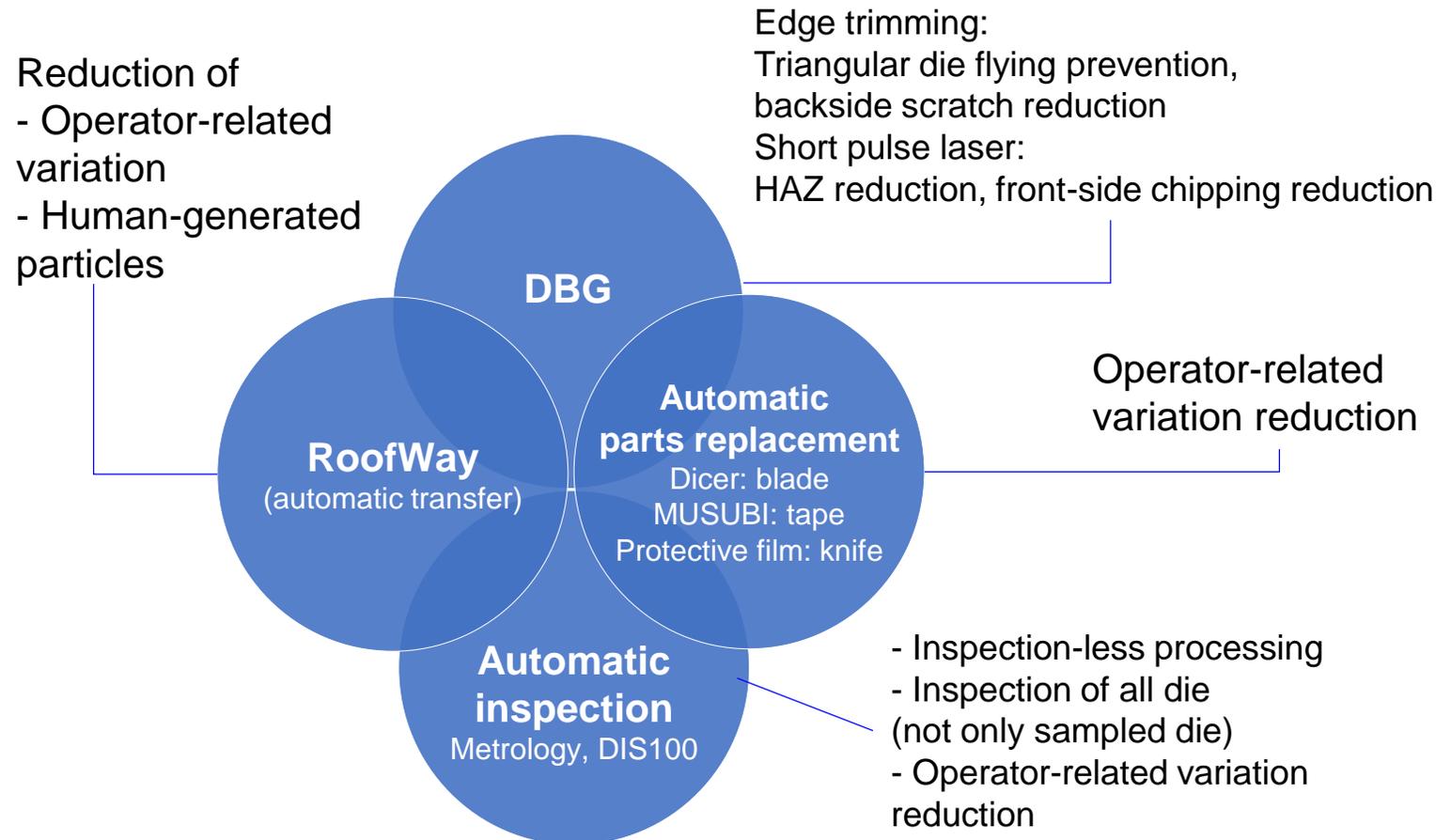
Quality-related demands  
for cutting-edge  
automotive logic ICs

**Zero Defects**

Minimization of defect occurrence and  
outflow risk

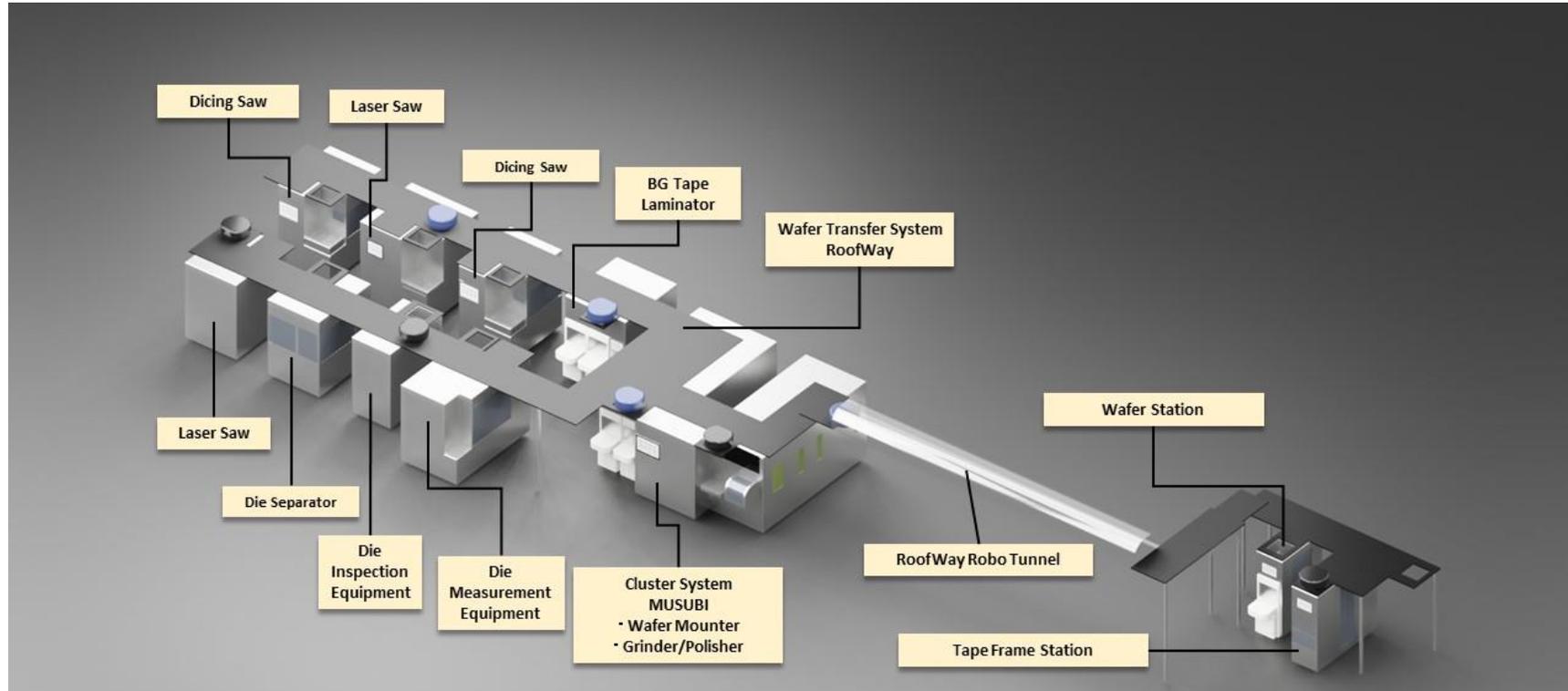
Maximization of process  
performance and quality stability

**Automation of production**



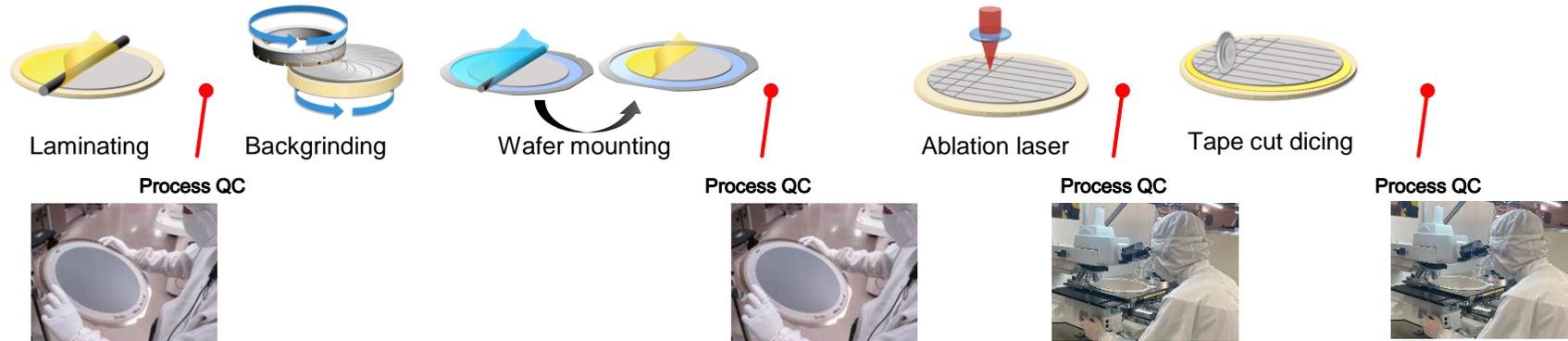
With utilization of these 4 elements, drastic reductions to and substitutions for routine operator work in clean rooms can be expected.

## Wafer transfer system RoofWay and cluster system MUSUBI are permanently installed at this center.



In this line, a fully-automatic transfer robot connects a series of processes, such as wafer thinning, dicer/laser singulation, 6-side die inspection and data storage after processing, etc.

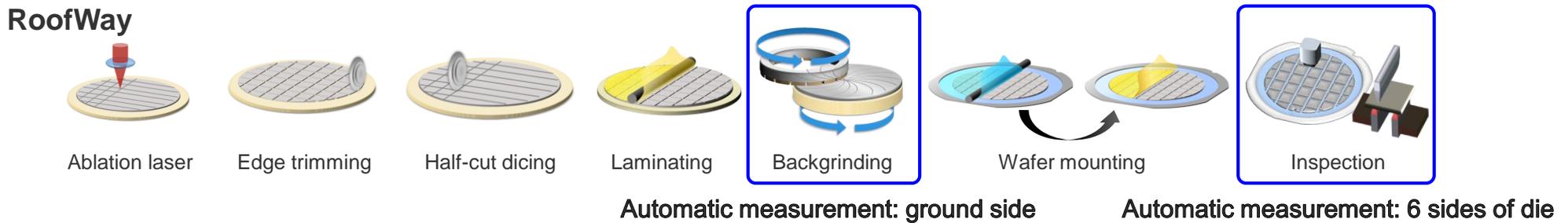
## Current Line: Logic Process



QC required

Limitations on reliability with operator-performed work

## Mid-Process: Logic DBG Process (Labor-Saving Line)



QC-less

Realization of a zero defect process

## Current line

## Mid-process

### Defect occurrence prevention

- Processing variation
- Human error
- Contamination, foreign materials, corrosion



- DBG process
- Short pulse laser
- Automation

### Defect outflow prevention

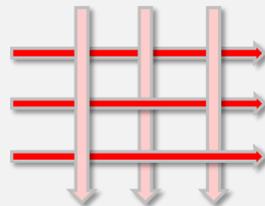
- Visual check
- Sampling check



- Quality check for all lines, all wafers (front-side and backside)
- Sidewall sampling check

### Defect outflow prevention

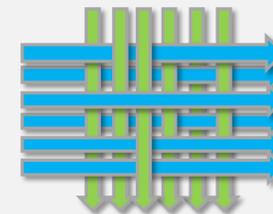
Defect occurrence prevention



Coarse quality filter

### Defect outflow prevention

Defect occurrence prevention



Fine quality filter

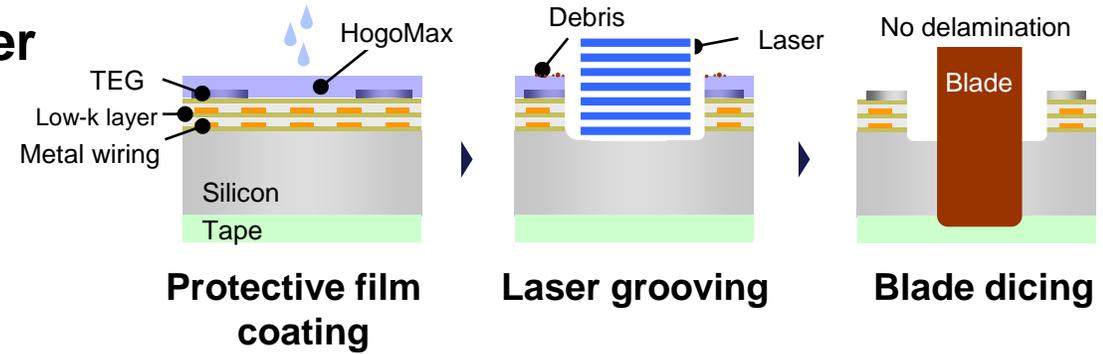
- **Laser grooving—produces minimal heat effects**
- **Edge trimming—eliminates defects caused by triangular die**
- **DBG process—produces less backside chipping**



**Maximized process performance**

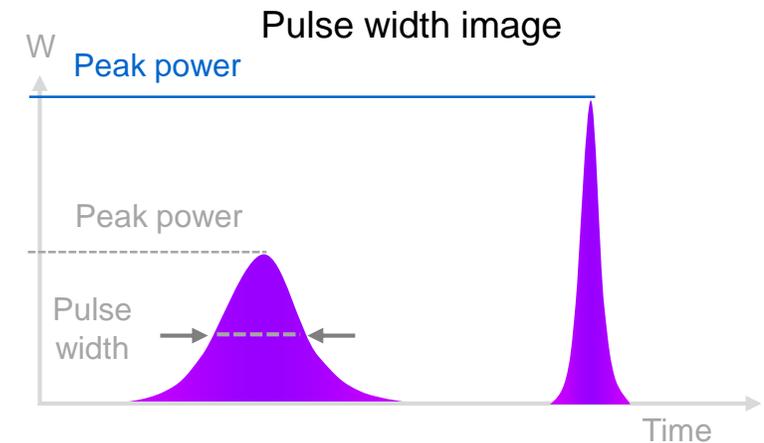
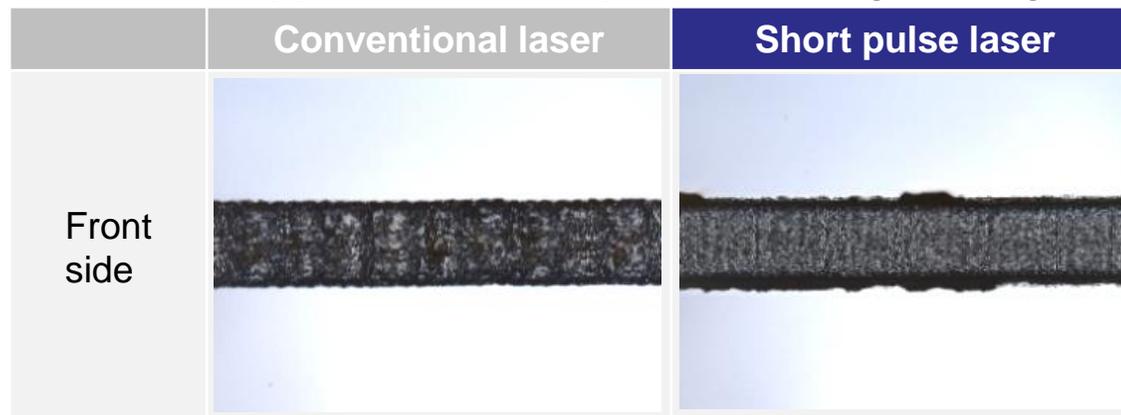
- **Removes the front side (patterned side) using a laser**
  - Generally, laser grooving is implemented to prevent interlayer dielectric film (low-k) delamination.

**Realizes stable processing quality not dependent on surface condition**

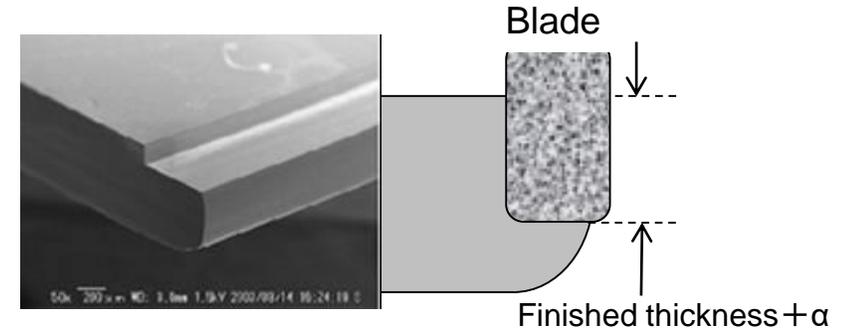


- **Reduces heat damage with ultrashort pulse laser**
  - Surface condition after laser grooving affects blade dicing

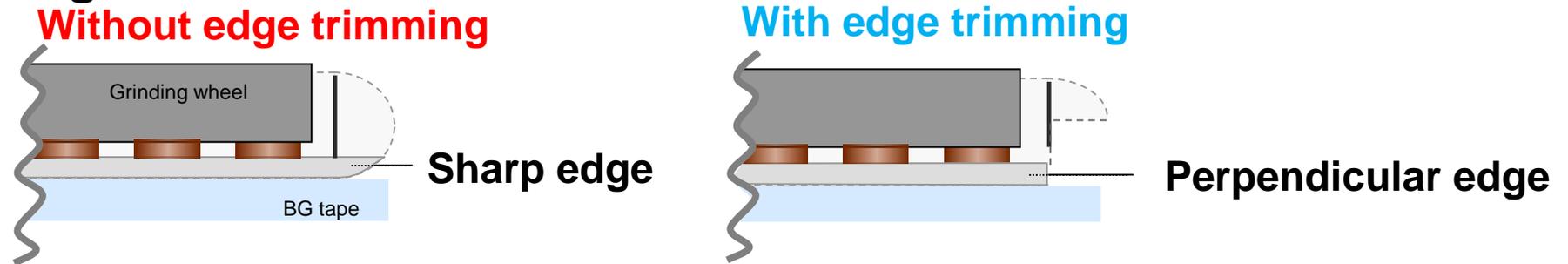
Application example: Si laser grooving



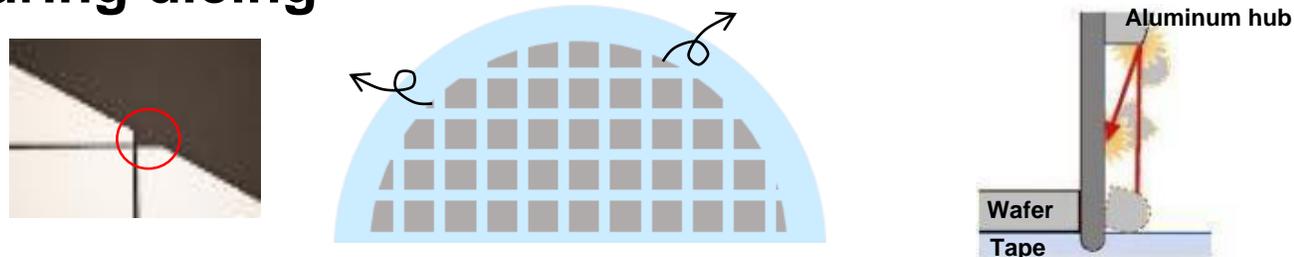
- Trims the wafer edge using a dicing blade before backgrinding



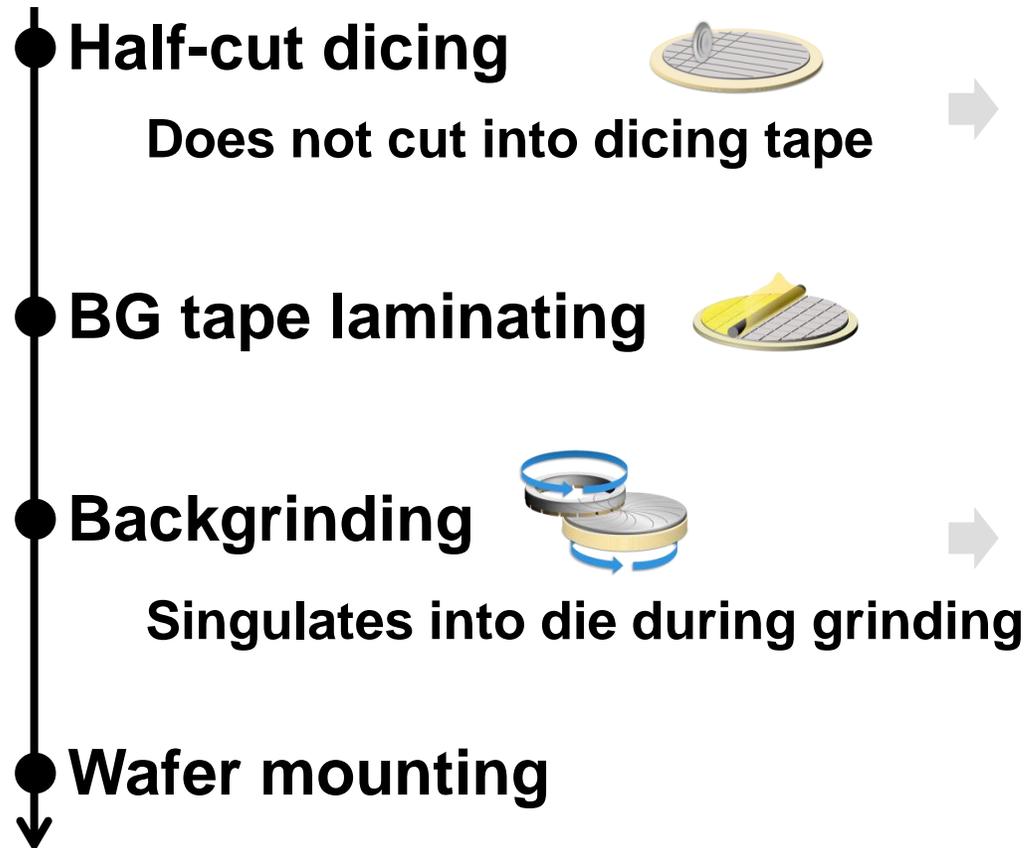
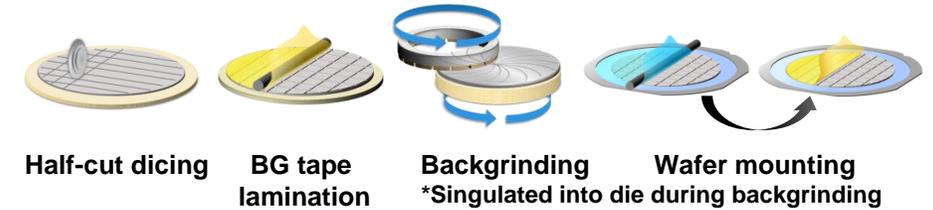
- Reduces sharp edges on wafer after thinning, preventing wafer breakage



- Reduces die damage and blade breakage due to triangular die flying during dicing



- Thinning after wafer half cutting (grooving)
- Prevents defects due to triangular die flying



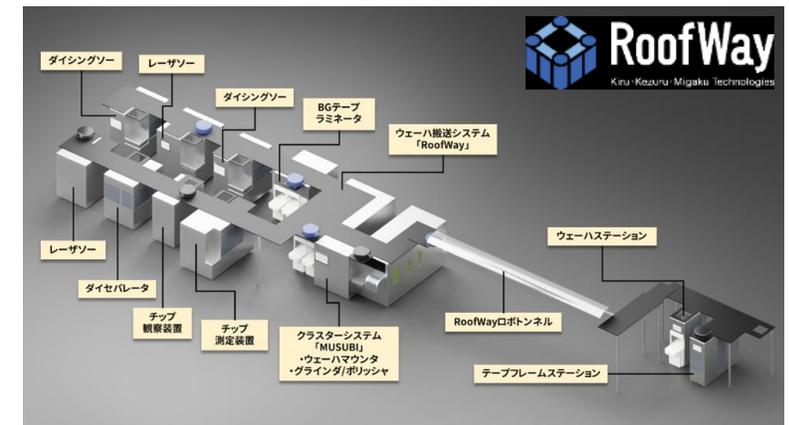
- No blade damage
  - Improved cutting speed
  - No need to adjust cutting position  
(kerf check reduction)
- 
- Good for backside chipping → die strength improvement
  - Street reduction possible without step cut

- **What is “variation”?**
  - “Variation” is a risk factor for human error-related defects.
    - Variation is difficult to eliminate even when countermeasures are taken, and the countermeasures themselves can become burdensome.
    - Other types of variation also exist, such as those related to parts and equipment.
- **How can we achieve variation-less processes?**
  - By reducing manned operation as much as possible through automation
    - Automation tools implemented at the Mid-Process Research Center
      - Remote-controlled operation, centralized data management (KKM-Link)
      - Automated transfer between equipment (RoofWay)
      - Automated tool replacement (blades)
      - Automated inspection (Metrology, DIS100)
    - Indirect benefits
      - Particle reduction
- **However, highly-reliable processes with high processing performance are also necessary.**
  - If operator intervention is required, the advantages of automation are reduced.

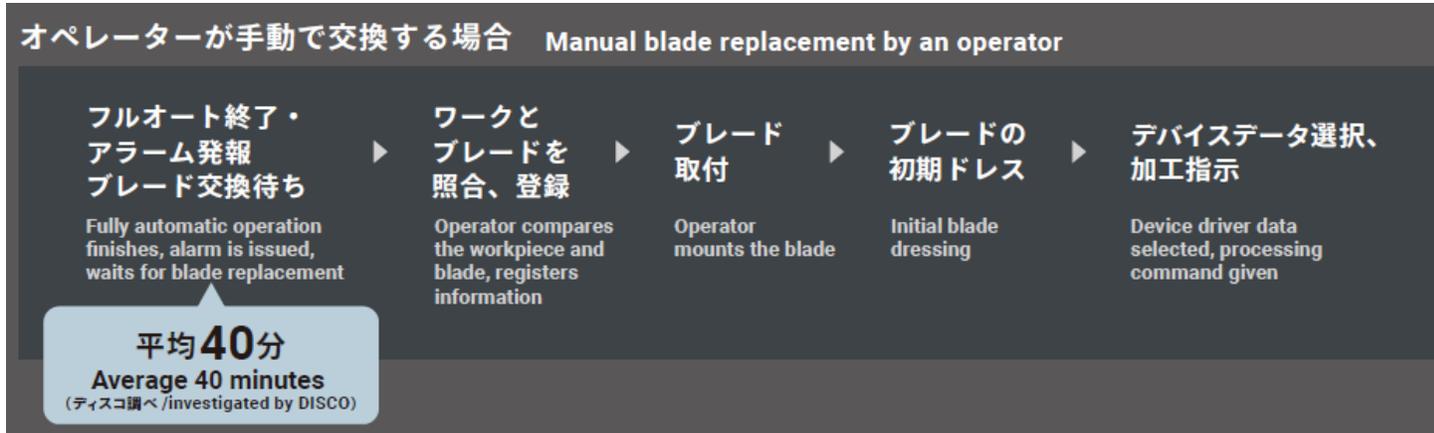




**Shortest TAT possible**  
(minimal time in clean room)



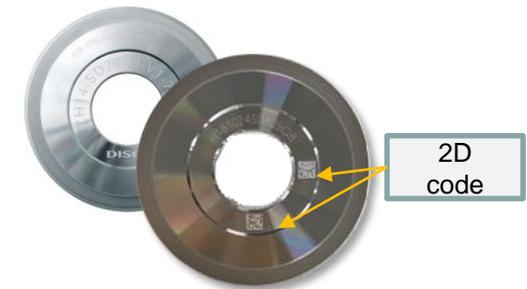
- **Downtime reduction through full automation of blade replacement and precutting**



	Conventional method	ABC
Concept		

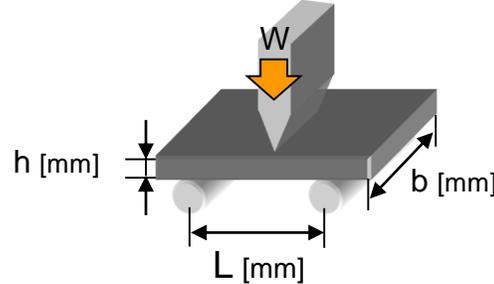
- 6 replacement blades stocked on each axis
- Scans 2D code on hub base to register blade information to equipment (patented)
  - Blade type
  - Actual kerf width (inspection data)
  - Actual blade exposure amount (inspection data)

- **Reduced operator-related blade replacement errors**
  - For example, incorrect blade type, blade tip breakage during mounting
- **Blade records management system**
  - To satisfy end-user quality assurance demands
- **Reduced blade cost**
  - Maintains records for used blades so that blades can be used to end of life



- Die measurement equipment that is fully automatic, from die picking to die strength measurement

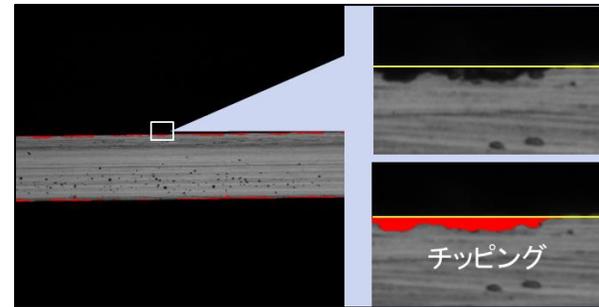
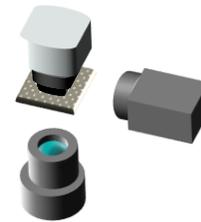
- Die strength measurement
  - 3-point bending test



$$\delta = \frac{3LW \times 9.8}{2bh^2}$$

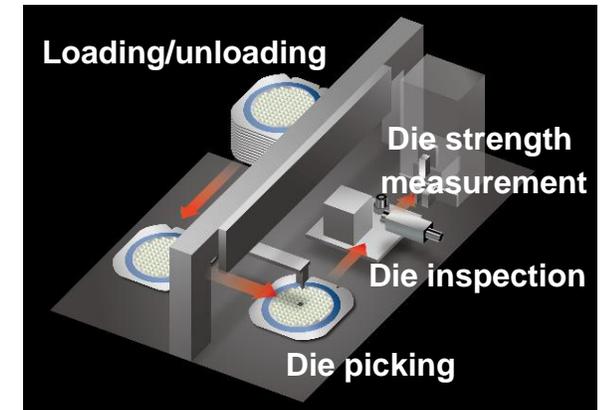
$\delta$ : Die strength [MPa]  
W: Breaking load [kgf]

- Supported inspection (options)
  - 4-point bending, ball-point bending test
  - Die backside inspection: surface roughness measurement
  - Die sidewall inspection
    - 1-point measurement: thickness measurement, chipping inspection
    - 4-side measurement



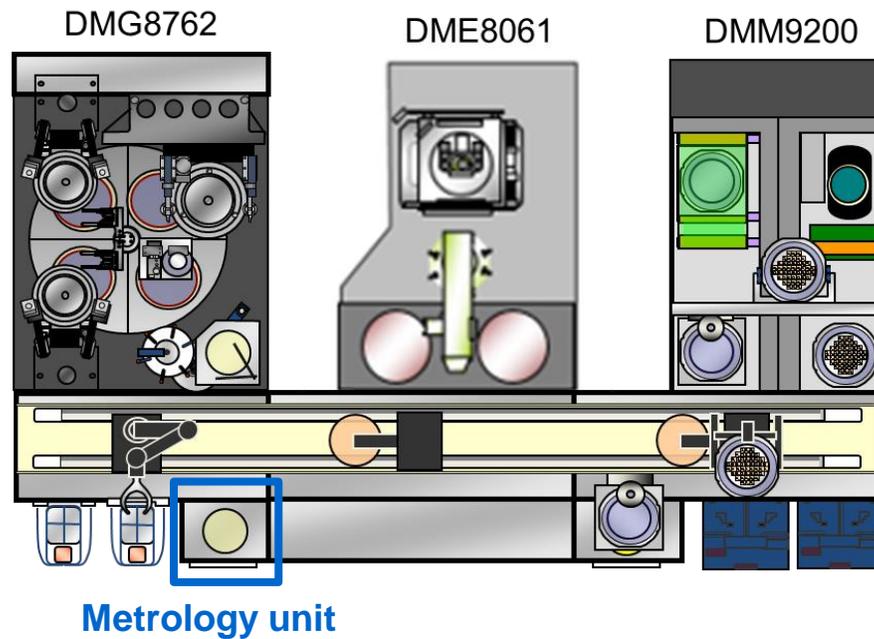
DIS100

## Equipment layout



W x D x H: 1,250 mm x 1,680 mm x 1,800 mm

- **Built-in metrology unit for MUSUBI for wafers after backgrinding**
  - Automated measurement of wafer condition after backgrinding
  - Possible to inspect all die, contributing to traceability



#### Main body functions

Thickness measurement  
(can be performed for individual die as well)

DBG/SDBG  
kerf recognition

Image capturing

- **Minimizes operator work through automation**
  - **Contributes to particle reduction in the process**
  
- **Automation means no cassette transfer between processes**
  - **Contributes to particle reduction by decreasing the number of times the cassette and frame come into contact**

- **Realizing zero defects as required by high value-added devices such as automotive devices**
  - **Maximized process performance + automation are required.**
    - **Highly-reliable processes (maximized process performance)**
      - **DBG**
      - **Short pulse laser**
    - **No variation (automated)**
      - **RoofWay / KKM-Link**
      - **Metrology**
      - **Automation tools (ABC, etc.)**

# Generative AI: 2.5D Packaging

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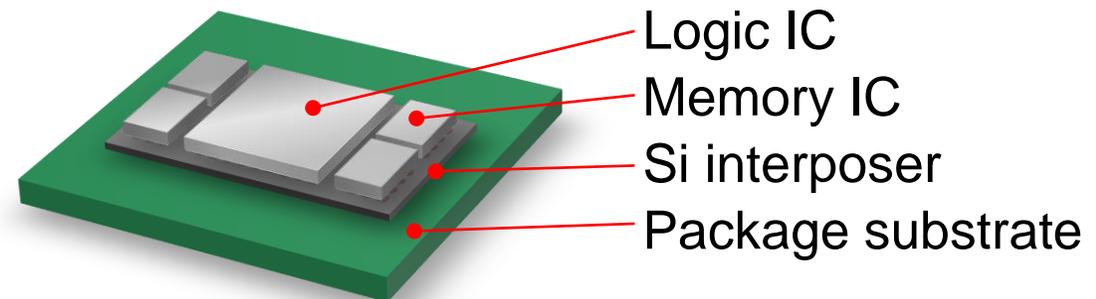
- Generative AI
  - What is “Generative AI”?
  - 2.5D Packaging
- KKM for 2.5D Packaging
  - Logic ICs
  - Memory ICs (HBM)
  - 2.5D Packaging
- Summary

\*The process flow described in this document is not a complete overview of all processes required for 2.5D packaging.

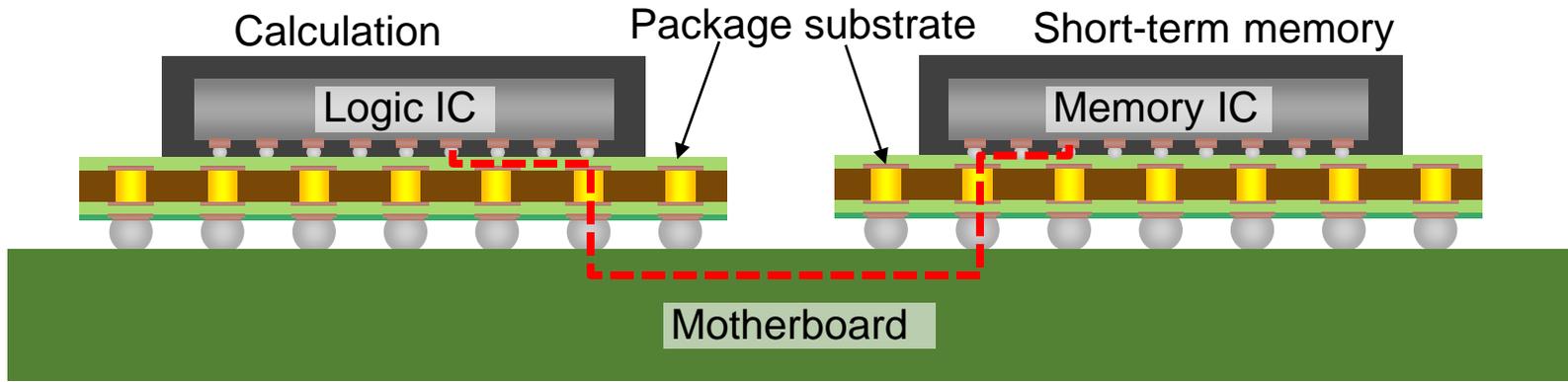
- Generative AI:  
one type of AI (Artificial Intelligence)



- Performance required for generative AI: high-speed, large-scale data processing and complex calculation  
→HPC (High Performance Computing)
- Packaging technology to realize HPC  
→2.5D packaging

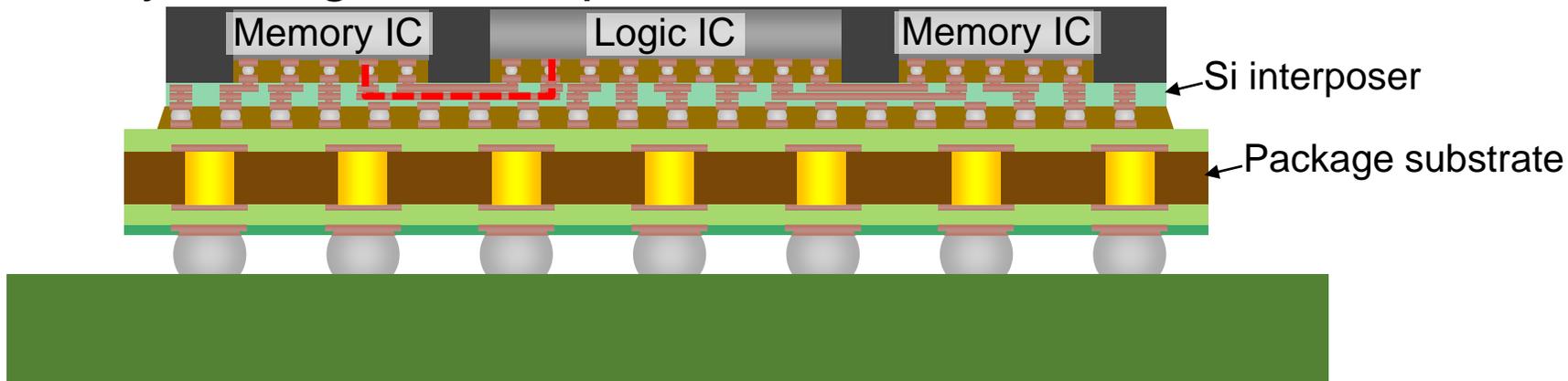


- Conventional Packaging: not suited for high-speed, large-scale calculations



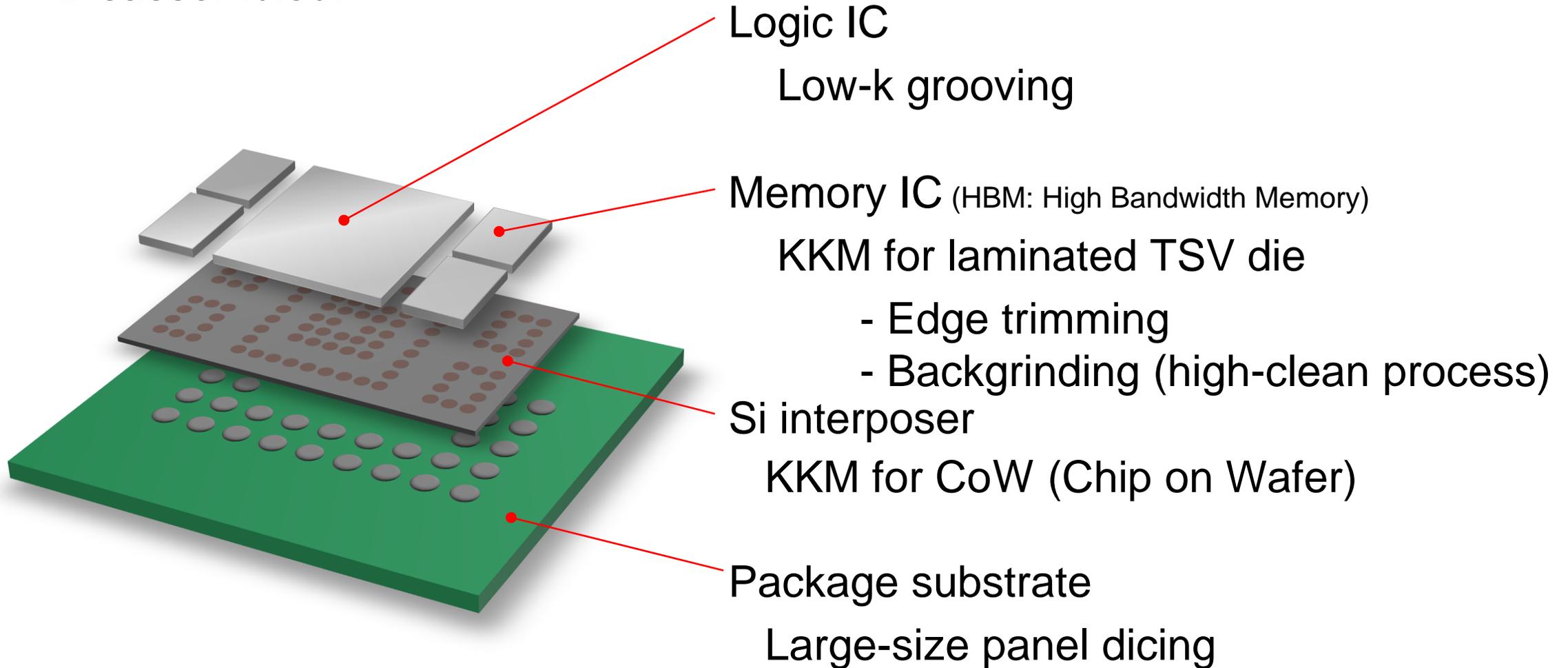
- Logic IC  
- Memory IC  
Packaged separately  
Connected through motherboard

- 2.5D Packaging: high-speed communication possible between logic ICs and memory through Si interposer



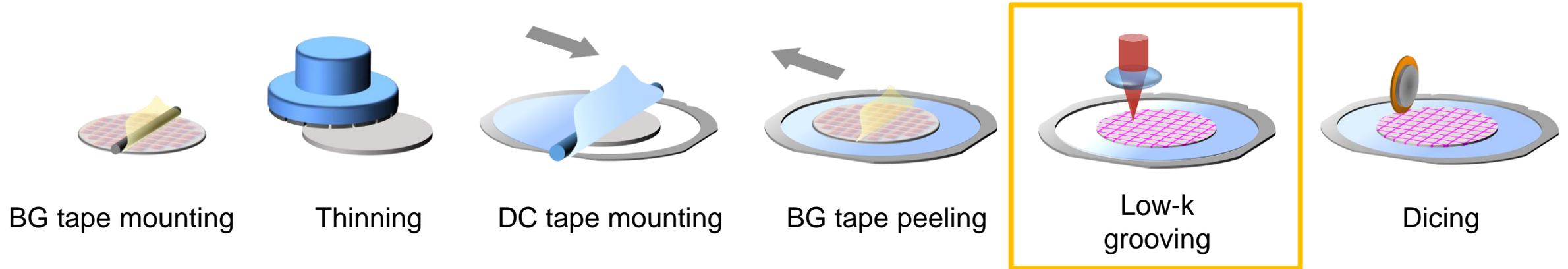
- Logic IC  
- Memory IC  
Packaged together  
Connected within package

- Disassembled:

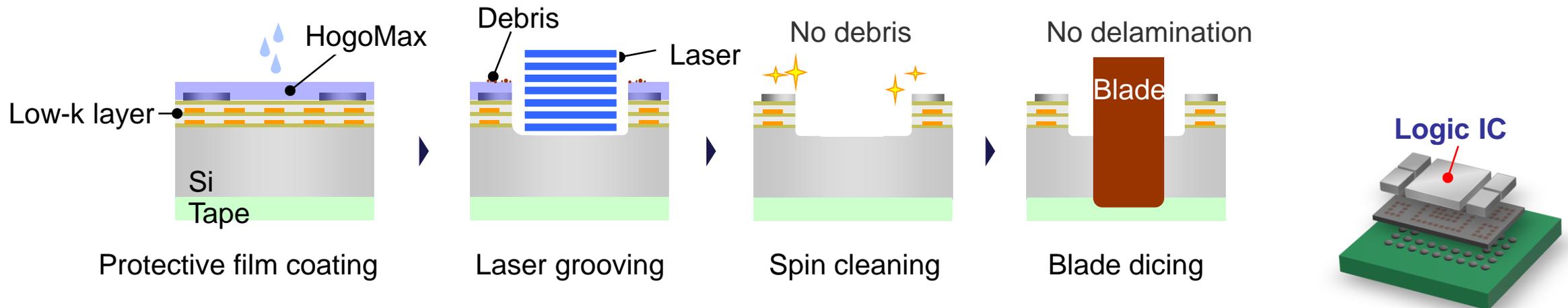


- Generative AI
  - What is “Generative AI”?
  - 2.5D Packaging
- KKM for 2.5D Packaging
  - Logic ICs
  - Memory ICs (HBM)
  - 2.5D Packaging
- Summary

- Low-k grooving added to the conventional singulation process



- Possible to process without low-k delamination through use of ablation laser

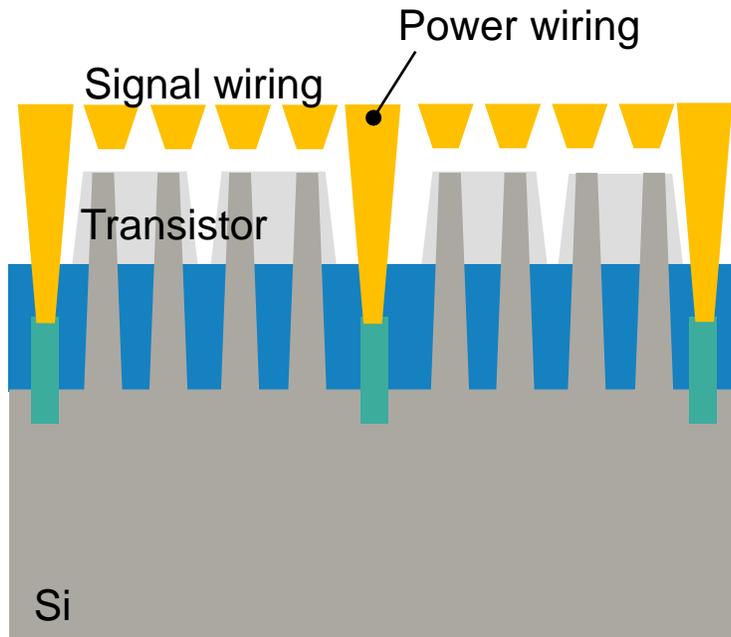


- Improvements to degree of integration for logic transistors: BS-PDN

Backside Power Delivery Network

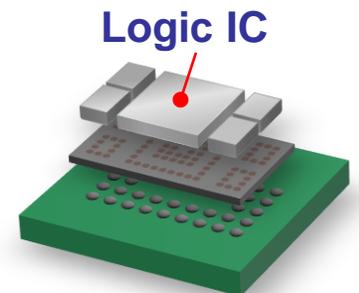
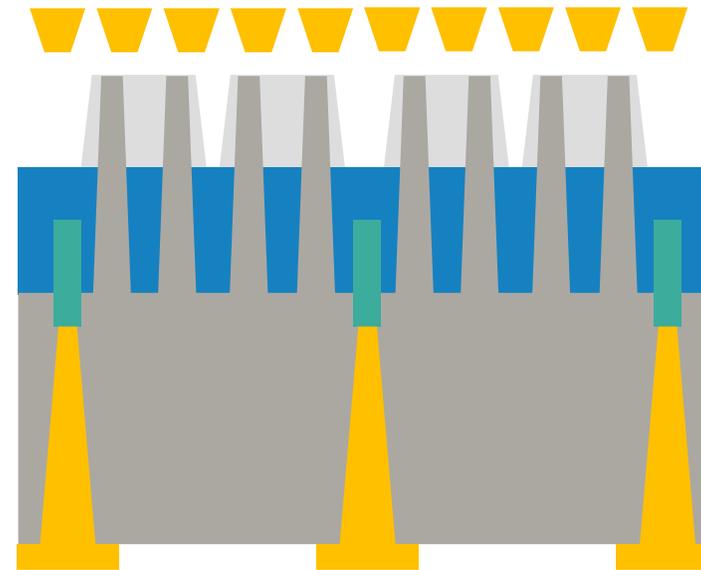
Conventional logic ICs:  
signal and power wiring on the surface

# of times thinning performed: 1  
Backgrinding of patterned wafer

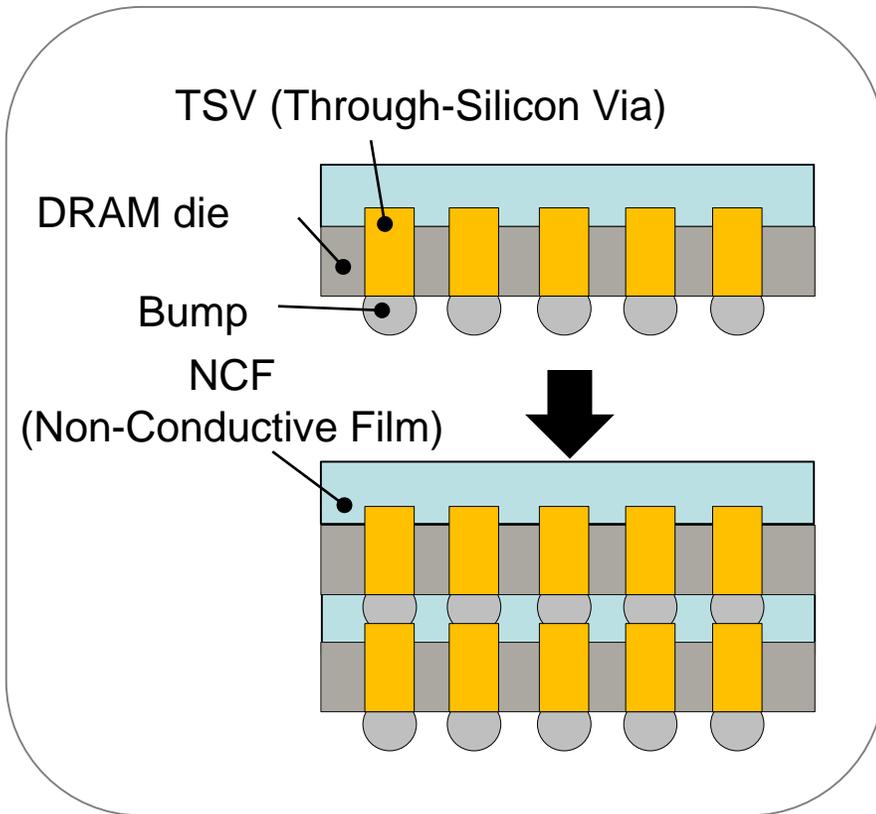


BS-PDN logic ICs:  
signal wiring on the surface, power wiring on the back

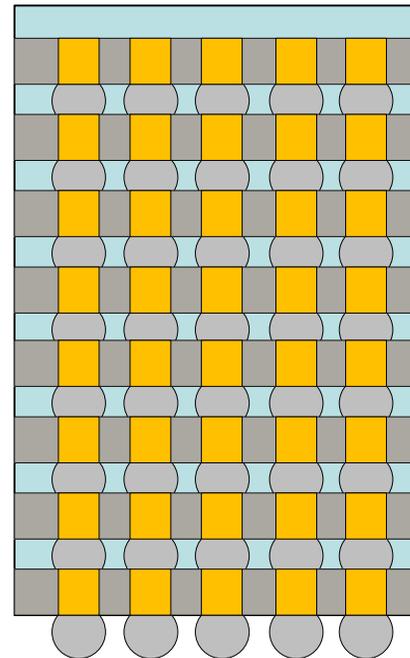
# of times thinning performed: 2  
- High-accuracy backgrinding of patterned wafer  
- Supports substrate grinding



- HBM (High Bandwidth Memory): DRAM die lamination using TSV

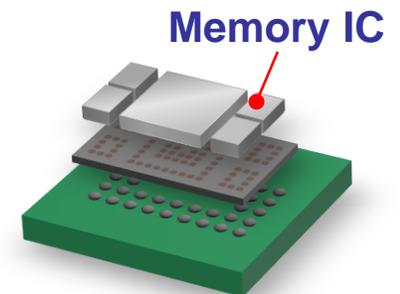


HBM  
8-layer laminated products



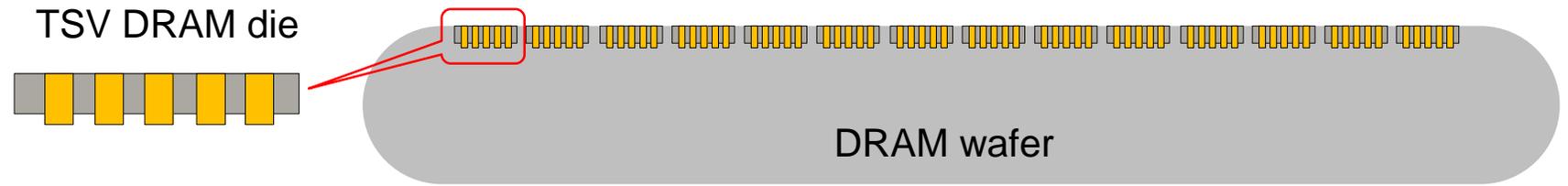
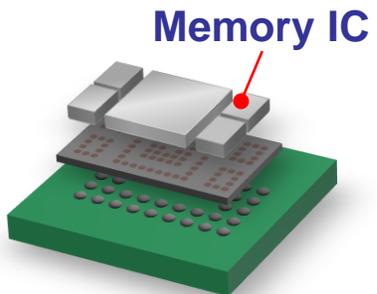
## Process

- Edge trimming
- Thinning (high-clean thinning)
- TSV reveal / bump formation
- Dicing
- Die lamination



## Process

- **Edge trimming**
- Thinning (high-clean grinding)
- TSV reveal / bump formation
- Dicing
- Die lamination



Edge trimming on wafer edge using blade dicing before thinning

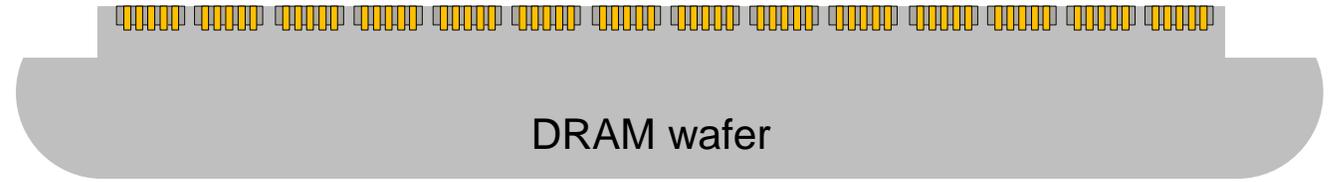
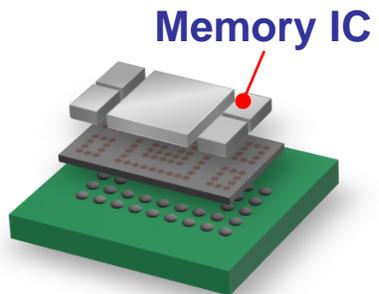


Without edge trimming  
Sharp edge during thinning,  
causing cracking and breakage

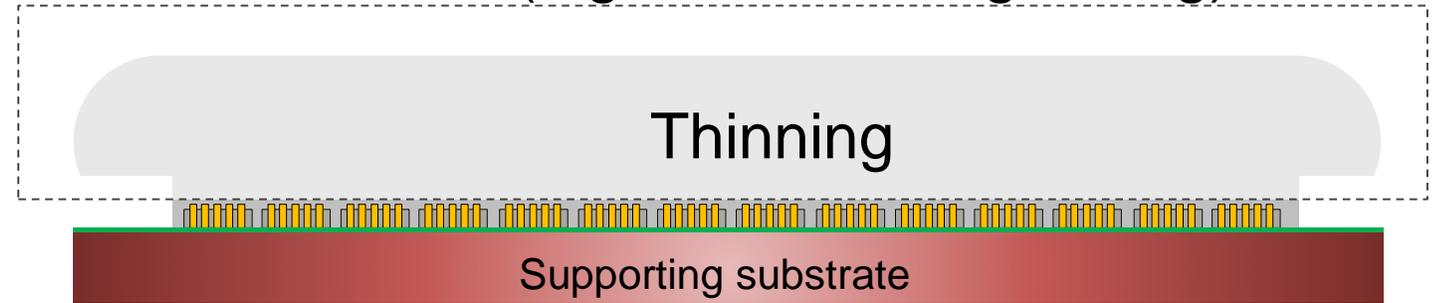
With edge trimming  
No sharp edge during  
thinning, reducing risk of  
cracking or breakage

## Process

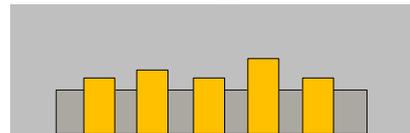
- Edge trimming
- **Thinning (high-clean grinding)**
- TSV reveal/bump formation
- Dicing
- Die lamination



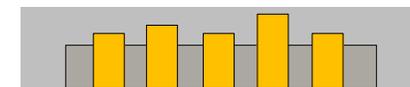
For handling in the next process, the wafer is thinned while temporarily bonded to the supporting substrate (high-clean backgrinding)



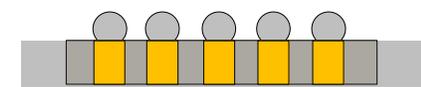
Before thinning  
With via height variation



After thinning

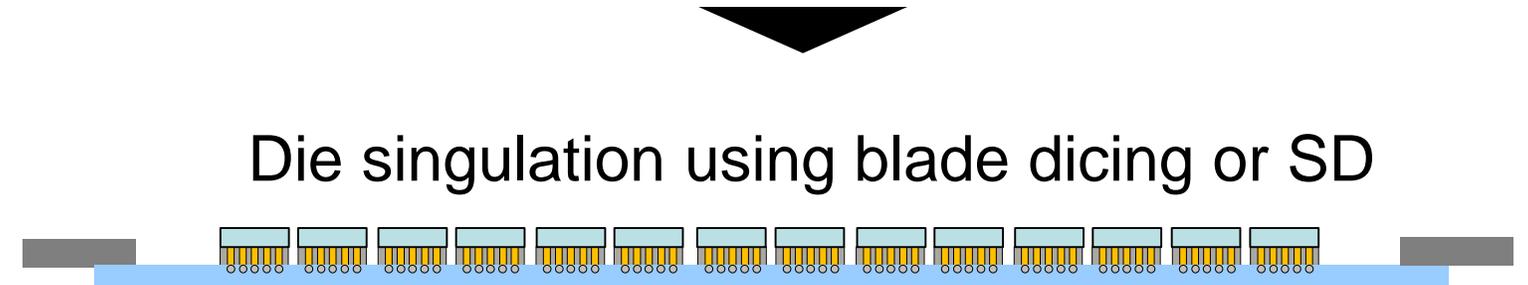
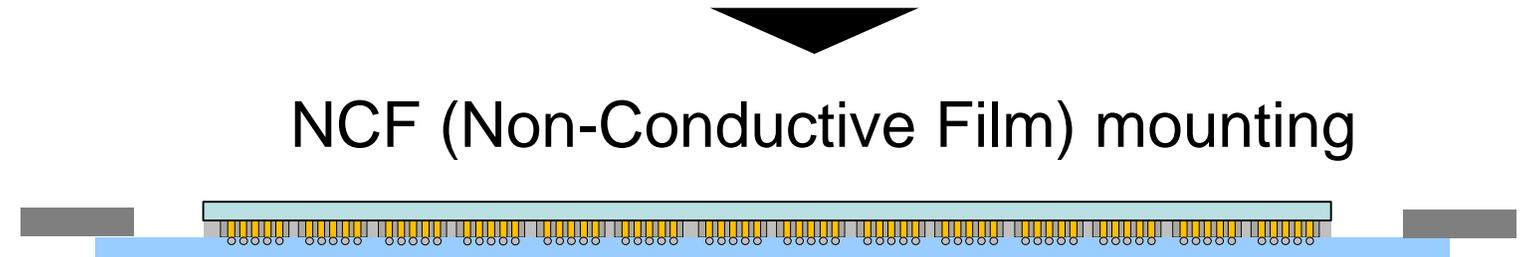
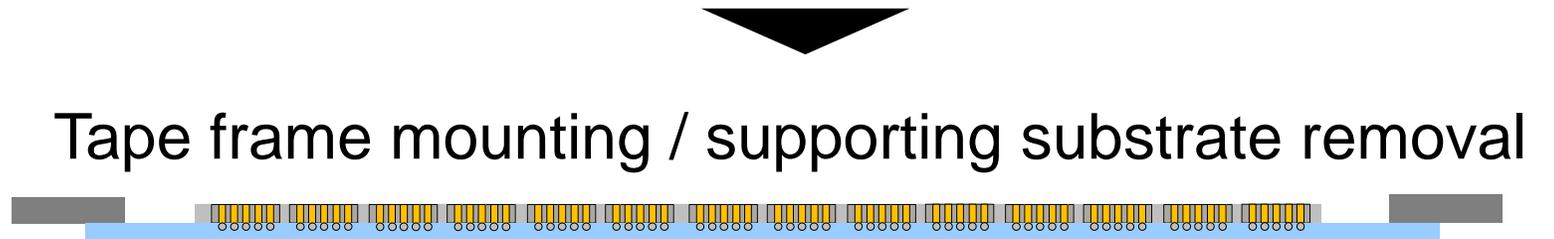
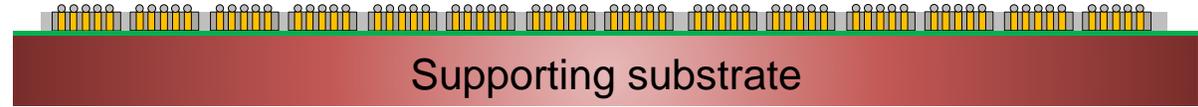
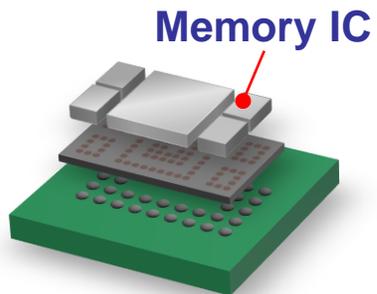


TSV reveal  
Bump formation



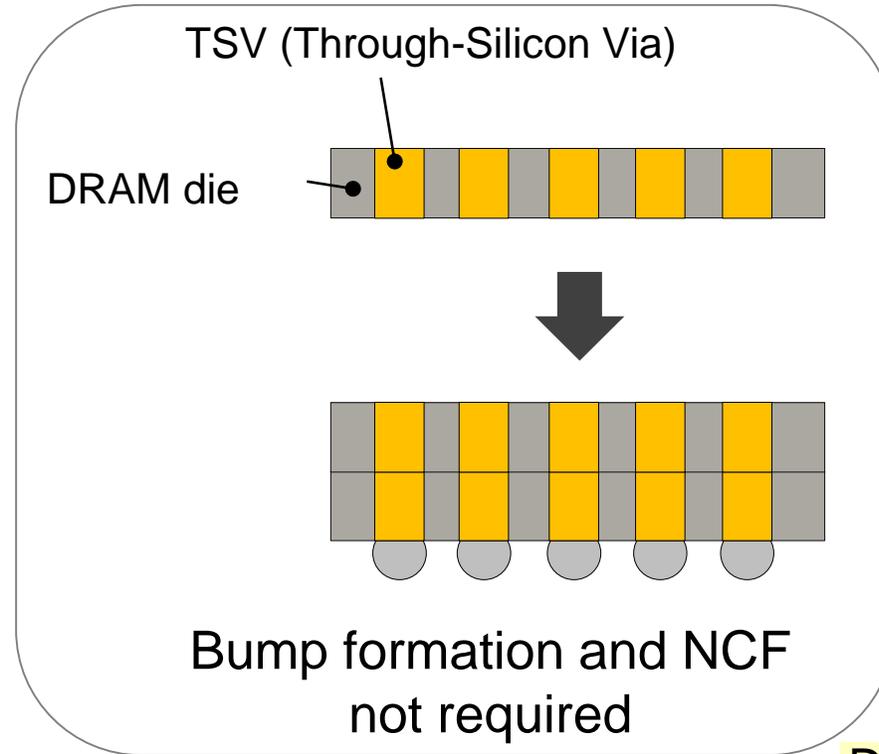
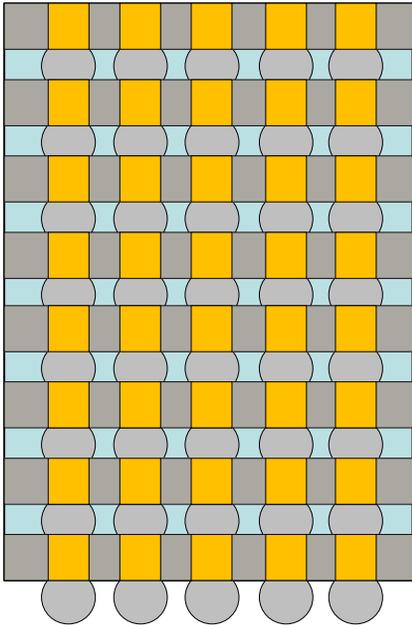
## Process

- Edge trimming
- Thinning (high-clean grinding)
- TSV reveal/bump formation
- **Dicing**
- Die lamination

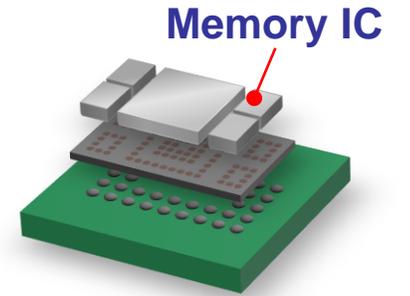
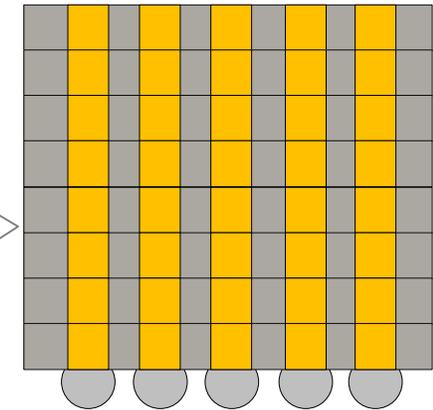


- Enabling die connection through hybrid bonding

## Bump connection



## Direct bonding



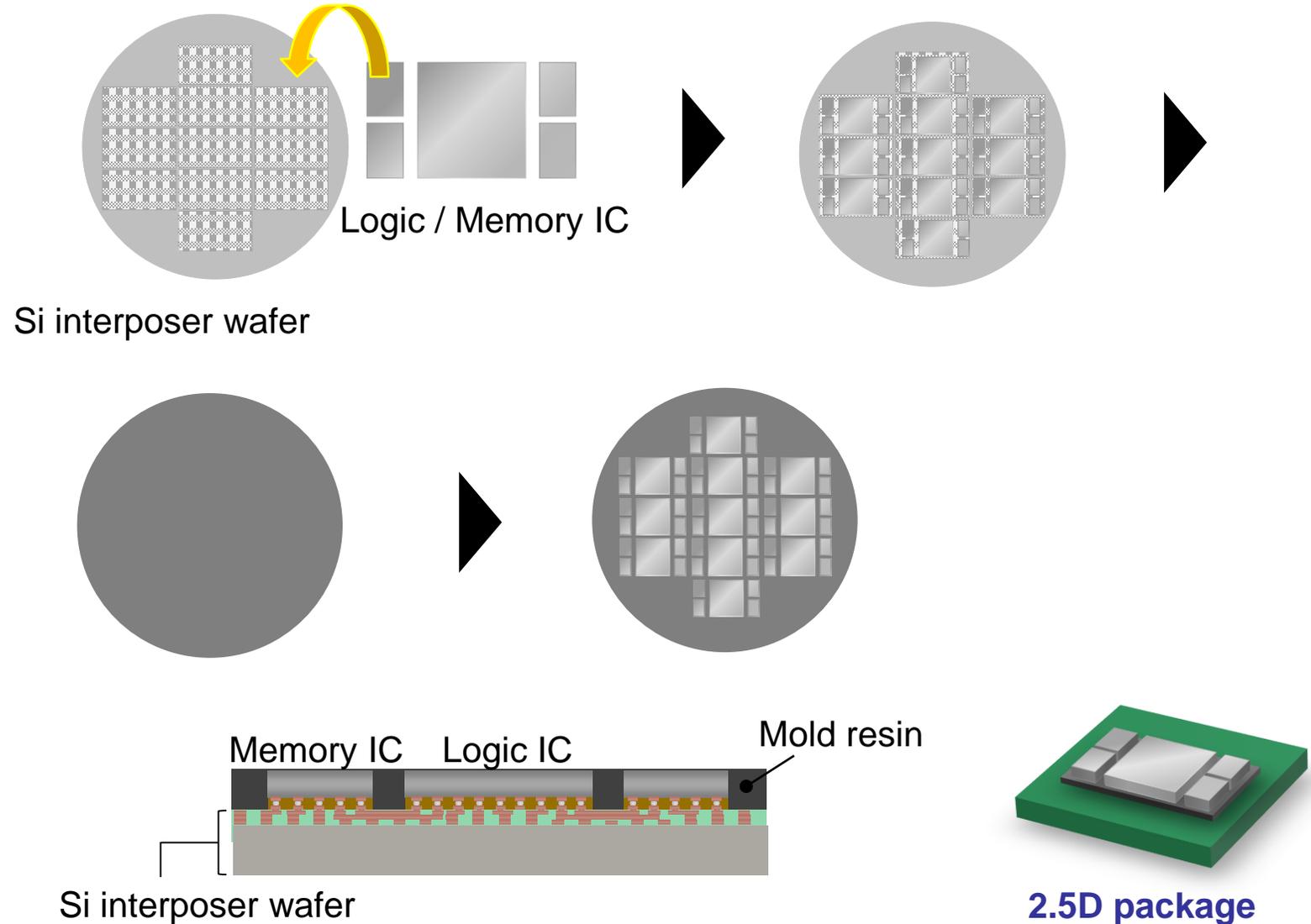
Demand for improvements to the following may increase.

- Processing quality of backgrinding finish
- Cleanliness after die singulation

- Generative AI
  - What is “Generative AI”?
  - 2.5D Packaging
- KKM for 2.5D Packaging
  - Logic ICs
  - Memory ICs (HBM)
  - **2.5D Packaging**
- Summary

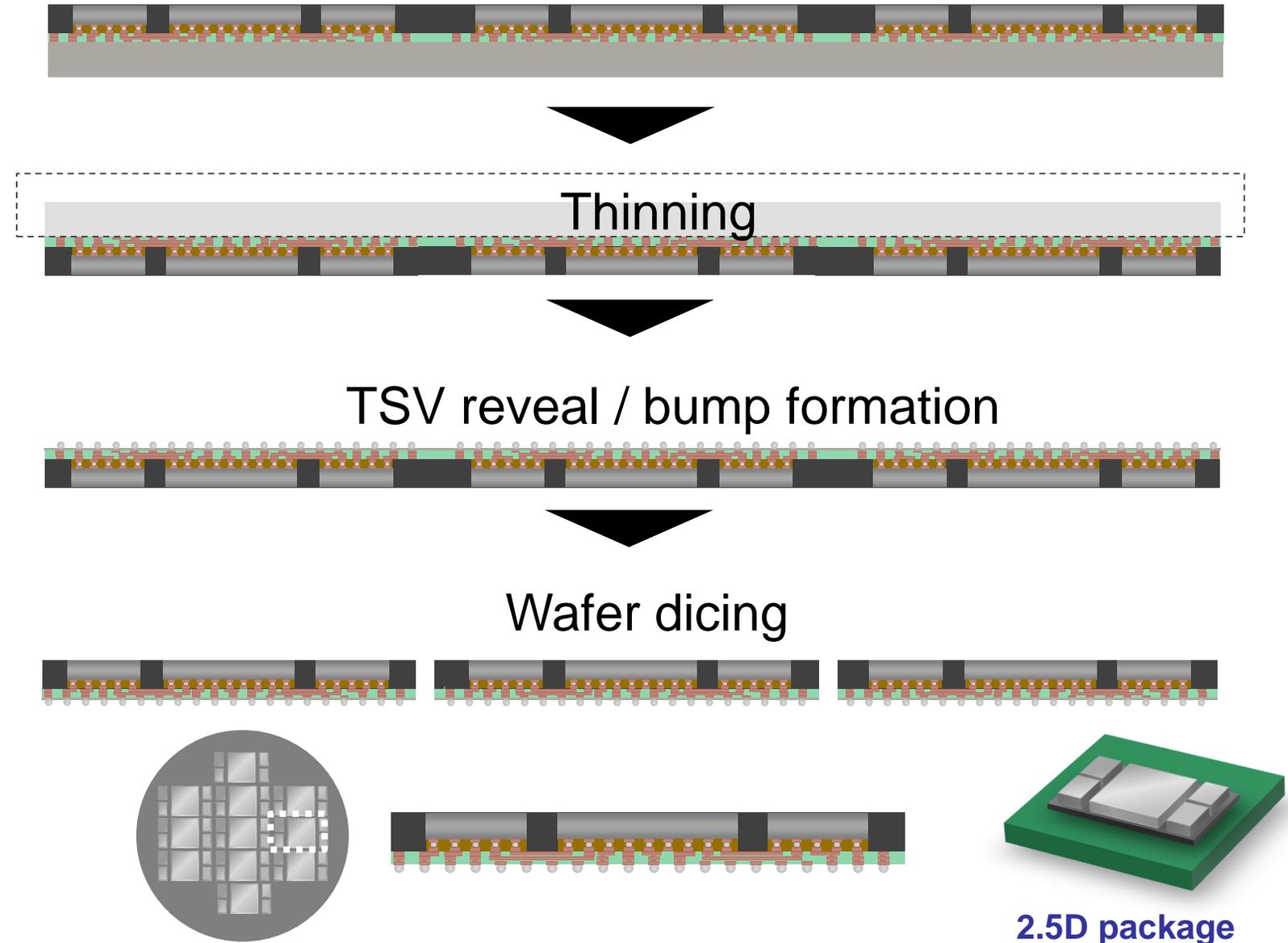
## Process

- Interposer wafer  
Logic/Memory IC installation
- Mold sealing
- Mold resin grinding
- Interposer thinning
- TSV reveal / bump formation
- Wafer dicing
- Mounting to package substrate
- Substrate dicing



## Process

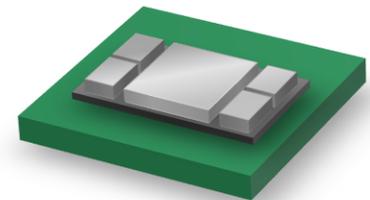
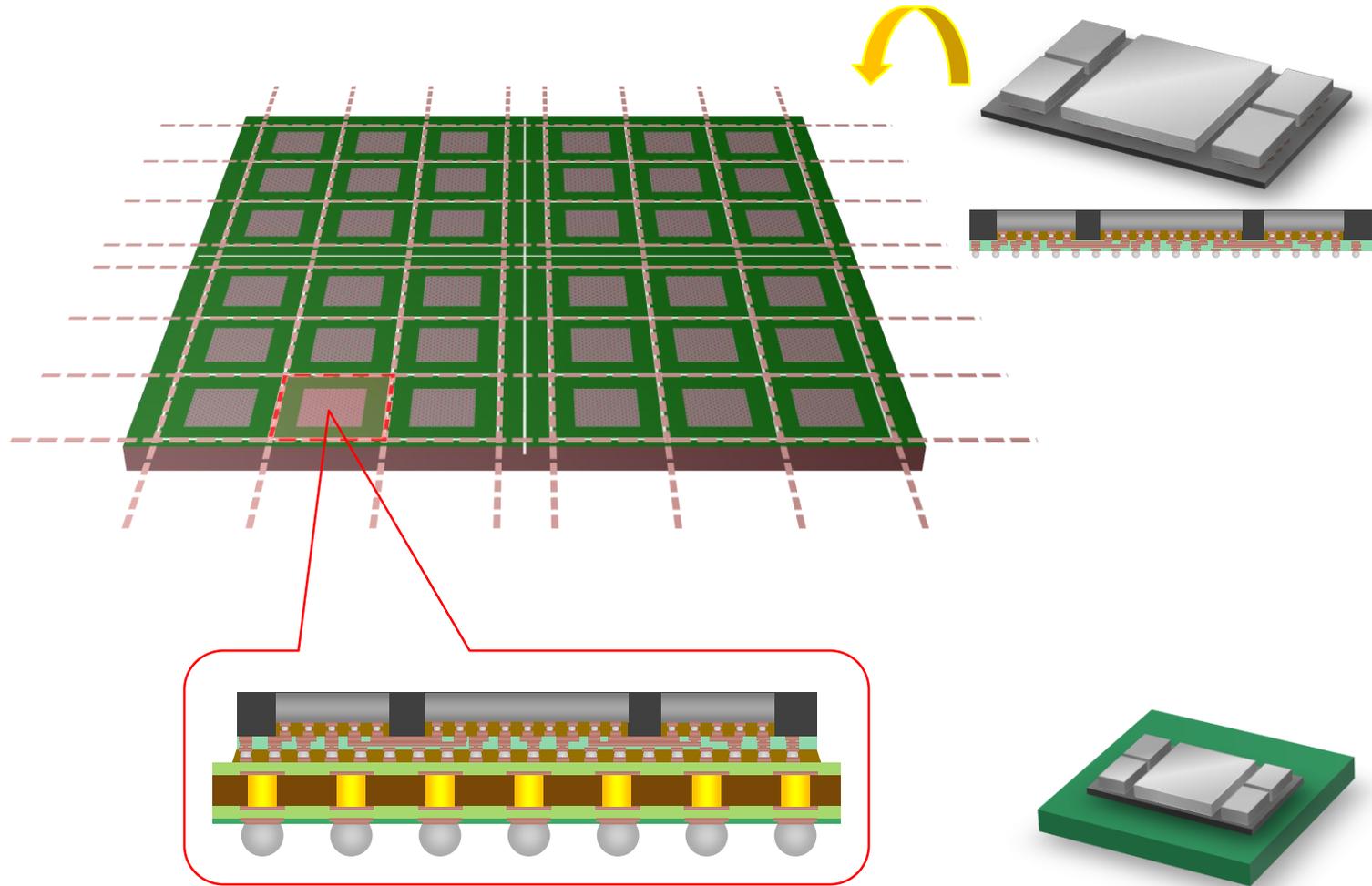
- Interposer wafer  
Logic/Memory IC installation
- Mold sealing
- Mold resin grinding
- Interposer thinning
- TSV reveal / bump formation
- Wafer dicing
- Mounting to package substrate
- Substrate dicing



2.5D package

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2.5D package

- Packaging technology for producing HPC for generative AI: 2.5D packaging technology
- 2.5D packaging: logic IC made into package by connecting logic and memory ICs using Si interposer
- Various types of KKM are being utilized for 2.5D packaging technology:
  - Low-k grooving
  - Edge trimming, backgrinding (high-clean process)
  - KKM for CoW (Chip on Wafer)
  - Large package dicing
- As BS-PDN and hybrid bonding evolve, further KKM expansion is expected.

### This material

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### Notation

The yearly accounting period from April of the current year to March of the following year is denoted by FY (Fiscal Year), and quarterly accounting periods are denoted by 1Q (April – June), 2Q (July – September), 3Q (October – December), and 4Q (January – March). Depending on the monetary unit, figures lower than the minimum unit may be rounded up or down, as a result of which the total sum may not match. Percentages are calculated based on the actual figures.

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